In the Claims:

1. (original) A circuit arrangement for operating at least one light-emitting diode (LED) in an electrical circuit at a service voltage (UB), which is greater than the forward voltage of the at least one light-emitting diode (LED) which is to be operated,

- wherein adjustment of the current flowing through the light-emitting diode (LED) is performed by means of pulse-width modulation of a first switching means (S1), which is switched between a first terminal of the service voltage (UB) and the light-emitting diode LED,
- wherein between the first terminal of the service voltage (UB) and the at least one light-emitting diode (LED) a first reactance formed by the first resistance (R1) and the first capacitor (C1) is arranged,

characterized in that

- the at least one light-emitting diode (LED) is connected via se second reactance formed by the second resistance (R2) and the first capacitor (C2) to the second terminal of the service voltage,
- between the two connections of the at least one light-emitting diode (LED) and the two reactances (R1-C1, R2-C2) a full-wave rectifier diode bridge of four diodes (D1, D2, D3, D4) being switched, and
- at a tap between the first switching means (s1) and the at least one light-emitting diode (LED) a connection, switchable via a second switching means (S2), to the second terminal of the service voltage

exists, the second switching means (S2) being operated in push-pull action to the first switching means (S1).

2. (original) A circuit arrangement according to claim 1, characterized in that the service voltage is a d.c. voltage and in that the service voltage is applied at the first terminal and the ground potential is applied at the second terminal and in that the full-wave rectifier circuit is formed of four diodes (D1, D2, D3, D4), the diodes being interconnected as follows:

- the first diode (D1) is polarized in forward direction and is switched between the first reactance (R1-C1) and the positive terminal (U_{LED+}) of the light-emitting diode (LED),
- the second diode (D2) is polarized in the inverse direction and is switched between the first reactance (R1-C1) and the negative terminal (U_{LED-}) of the light-emitting diode (LED),
- the third diode (D3) is polarized in forward direction and is switched between the second reactance (R2-C2) and the negative terminal (U_{LED-}) of the light-emitting diode (LED),
- the fourth diode (D4) is polarized in the inverse direction and is switched between the second reactance (R2-C2) and the positive terminal (U_{LED+}) of the light-emitting diode (LED).

3. (original) A circuit arrangement according to claim 2, characterized in that for level adaptation, the pulse-width modulated signal (PWM) is connected to the basis of a level

transistor (T0) of the circuit arrangement, of which the collector is connected to the ground (GND) and its emitter is connected to the service voltage (UB) as well as to the bases of a first White's emitter follower for the purpose of current amplification, which first White's emitter follower is substantially composed of a first NPN transistor (T1) and a first PNP transistor (T2), the emitter of the NPN transistor (T1) being connected to the emitter of the PNP transistor (T2) and to the first resistance (R1), and the collector of the NPN transistor (T1) being connected to the service voltage (UB), and the collector of the PNP transistor (T2) being connected to the ground (GND).

4. (original) A circuit arrangement according to claim 3, characterized in that for limiting the rise time of the signal (PWM) modulated in pulse-width, and amplified in current, a second White's emitter follower from a second NPN transistor (T3) and a second PNP transistor (T4) is connected between the first resistance (R1) and via a further resistance (R0) to the emitter of the first White's emitter follower, between the further resistance (R0) and the bases of the second White's emitter follower a second capacitor (C0) being connected to the ground (GND).

Claim **5** (canceled).

6. (new) A circuit arrangement according to claim 1, characterized in that the level transistor (T0) and/or the first NPN transistor (T1) and/or the first PNP transistor

(T2) and/or the second NPN transistor (T3) and/or the second PNP transistor (T4) are embodied as metal-oxide field-effect transistors.

7. (new) A circuit arrangement according to claim 2, characterized in that the level transistor (T0) and/or the first NPN transistor (T1) and/or the first PNP transistor (T2) and/or the second NPN transistor (T3) and/or the second PNP transistor (T4) are embodied as metal-oxide field-effect transistors.

8. (new) A circuit arrangement according to claim 3, characterized in that the level transistor (T0) and/or the first NPN transistor (T1) and/or the first PNP transistor (T2) and/or the second NPN transistor (T3) and/or the second PNP transistor (T4) are embodied as metal-oxide field-effect transistors.

9. (new) A circuit arrangement according to claim 4, characterized in that the level transistor (T0) and/or the first NPN transistor (T1) and/or the first PNP transistor (T2) and/or the second NPN transistor (T3) and/or the second PNP transistor (T4) are embodied as metal-oxide field-effect transistors.

[REMARKS FOLLOW ON NEXT PAGE]